REMARKS

Claims 1 and 3-12 were examined and reported in the Office Action. Claims 1 and 3-12 are rejected. Claims 5, 7-8 and 11-12 are canceled. Claims 1, 6 and 9 are amended. Claims 1, 3-4, 6 and 9-10 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. In the Drawings

It is asserted in the Office Action that Figures 6-7 include connections that are not supported. Applicant respectfully disagrees.

Applicant notes that on page 6, lines 10-15 of the specification it is asserted that the "peak value sensor senses the maximum and/or minimum levels from the two outputs.... The error amplifier amplifies a difference between the detected maximum and minimum levels ...." Therefore, the connections between the peak value sensor and the error amplifier can be sufficiently derived from the foregoing. Approval is respectfully requested.

II. Claim Objections

It is asserted in the Office Action that claims 5 and 9 are objected to for informalities. Applicant has canceled claim 5. Applicant has amended claim 9 to overcome the informal objections.

Accordingly, withdrawal of the informal objection for claims 5 and 9 are respectfully requested.

III. 35 U.S.C. § 103(a)

A. It is asserted in the Office Action that claims 1 and 3-4 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent Pub. No. 2002/0109075 by Ono ("Ono") in view of U. S. Patent Application No. 5,955,921 issued to Ide et al. ("Ide").

According to MPEP §2142

> [t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that 'rejections on obviousness cannot be sustained with mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.' *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). See also *KSR*, 550 U.S. at __, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval).

Further, according to MPEP §2143, "[T]he Supreme Court in *KSR International Co. v. Teleflex, Inc.* 550 U.S. ___, ___, 82 USPQ2d 1395-1397 (2007) identified a number of rationales to support a conclusion of obviousness which are consistent with the proper "functional approach" to the determination of obviousness as laid down in *Graham*." Further, according to MPEP §2143.01, [o]bviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006). Further, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art." *KSR International Co. v. Teleflex, Inc.* 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007). Additionally according to MPEP §2143,

> [a] statement that modification of the prior art to meet the claimed invention would have been "well within the ordinary skill of the art at the time the claimed invention was made" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Pat. App. & Inter. 1993).

Ono discloses a DC cancellation circuit that cancels a DC offset voltage occurring between a pair of complimentary differential output signals output from a differential

amplification circuit. Referring to Fig. 1 of Ono, the I-V is double-ended, while the output of the I-V 42 is single-ended in Fig. 4 of Applicant's claimed invention.

Ide discloses a signal amplifier circuit that operates to reduce distortion of a pulse width caused that is due to input offset when a pulsed signal is reproduced. Referring to Fig. 1 of Ide, the output of the amplifier 3 is single-ended, while the output of amplifier 432 is double-ended, namely single-to-doubled in Fig. 5 of Applicant's claimed invention.

Even if the disclosure of Ide is added to that of Ono, the resulting invention would still not teach, disclose or suggest Applicant's amended claim 1 limitations of

> a peak value sensor which detects the maximum or minimum levels from the outputs of a limiting amplifier; and an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier, wherein intrinsic offsets and offsets inherited from a signal output from the differential amplifier are canceled if DC gain from the error amplifier is greater than a DC gain of the limiting amplifier, and the post amplifier comprises a series of sets, each of the sets comprising: a the limiting amplifier which amplifies the differential signals and cancels offsets inherited from the differential signals or an offset occurring during the amplification according to a predetermined control signal wherein the differential signals is are output from the single-to-differential converter for the first set and output from the limiting amplifier of the previous set for the subsequent sets; and a cascaded set of a plurality of auto-offset cancellation portion which calculates a difference between outputs of the limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the limiting amplifier, wherein the auto-offset cancellation portions comprises: the peak value sensor; and the error amplifier

Further, the assertions made in the Office Action on pages 4-5 that lead to a conclusion of obviousness are not explicit and the basic requirements of an articulated rationale under MPEP 2143 cannot be found. Additionally, since neither Ono, Ide, and therefore, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 1, as listed above, Applicant's amended claim 1 is not obvious over Ono in view of Ide since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 1, namely claims 3-4, would also not be obvious over Ono in view of Ide for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1 and 3-4 are respectfully requested.

B. It is asserted in the Office Action that claims 5-12 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Ono in view of Ide, and further in view of U. S. Patent Application No. 6,018,407 issued to Hatakeyama et al. ("Hatakeyama").

Referring to Fig. 2 in Hatakeyama, block OC(0) operates like a gain controller sine the outputs of PRE are fed back to the current sources, while S2D converter 43 feeds forward the output of the preamplifier, namely I-V 42. Further, Hatakeyama concerns arranging time constants between AOC blocks in an optical receiver so that the AOC works smoothly. Distinguishable, Applicant's claimed invention concerns a burst-mode receiver, without mention of a time constant. Hatakeyama at col. 5, line 55 to col. 6, line 17 discloses information regarding the time constant in the AOC block. Even though the idea of feedback to cancel offset is similar, the details are not described. This idea was proposed a long time ago, and the explanation is merely for understanding of the total circuit. Even though Hatakeyama mentions an ATC using top and bottom hold circuits, the topologies are quire distinguishable. Applicant's topology using S2D and consecutive AOC to solve the burst-mode receiver requirements is not taught, disclosed or suggested by neither Ono nor Hatakeyama.

Even if the disclosure of Hatakeyama is combined with that of Ono and Ide, the resulting invention would still not teach, disclose or suggest Applicant's amended claim 1 limitations of

> a peak value sensor which detects the maximum or minimum levels from the outputs of a limiting amplifier; and an error amplifier which amplifies the difference between the maximum or minimum levels and feeds an amplification result to the limiting amplifier, wherein intrinsic offsets and offsets inherited from a signal output from the differential amplifier are canceled if DC gain from the error amplifier is greater than a DC gain of the limiting amplifier, and the post amplifier comprises a series of sets, each of the sets comprising: a the limiting amplifier which amplifies the differential signals and cancels offsets inherited from the differential signals or an offset occurring during the amplification according to a predetermined control signal wherein the differential signals is are output from the single-to-differential converter for the first set and output from the limiting amplifier of

> the previous set for the subsequent sets; and a cascaded set of a plurality of auto-offset cancellation portion which calculates a difference between outputs of the limiting amplifier, amplifies the difference, and provides the amplification result as the predetermined control signal to the limiting amplifier, wherein the auto-offset cancellation portions comprises: the peak value sensor; and the error amplifier

Further, the assertions made in the Office Action on pages 5-7 that lead to a conclusion of obviousness are not explicit and the basic requirements of an articulated rationale under MPEP 2143 cannot be found. Additionally, since neither Ono, Ide, Hatakeyama, and therefore, nor the combination of the three, teach, disclose or suggest all the limitations of Applicant's amended claim 1, as listed above, Applicant's amended claim 1 is not obvious over Ono in view of Ide and further in view of Hatakeyama since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 1, namely claims 6 and 9-10 (claims 5, 7-8 and 11-12 being canceled), would also not be obvious over Ono in view of Ide, and further in view of Hatakeyama for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 5-12 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1, 3-4, 6 and 9-10 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: November 19, 2007

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 11/19/07
Suzanne Johnston Date: November 19, 2007